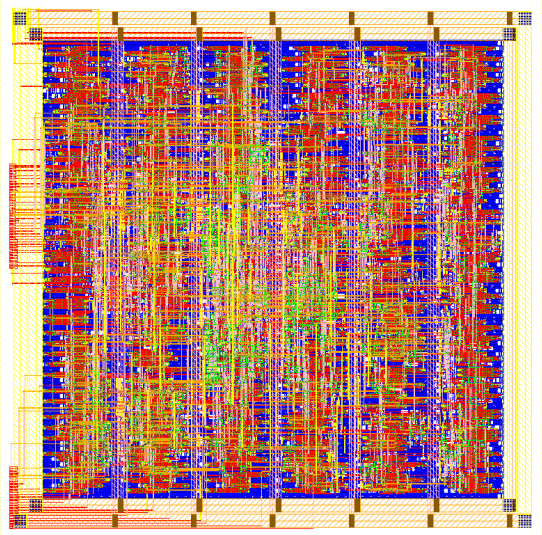
cogenda Integrated Solutions for EDA / TCAD / RadHard

RadHard IP and Design Services

- RadHard IP
  - Standard Cell and IO Library
  - Embedded SRAM
- Design Services
  - ASIC development
  - IP development
  - EDA flow integration



Standard Cell Library

Category	Description
Process Platform	- 0.13 um 1P8M CMOS - Epi-wafer not required - portable to similar foundry processes
Core Cell Library	- 114 cells of 35 types - SEU/SET hardened DICE flipflops - Cell height : 10 track - Gate density : 125k/mm^2
IO Cell Library	- 20 digital and analog cells - Cell height/pitch : 211 um / 50 um - 3.3 V LVCMOS - HBM ESD tolerance > 2000 V
EDA Views	- Liberty (.lib) for synthesis @ 5 PVT corners - Verilog simulation model - LEF and Milkyway for P&R - GDSII layout - LVS netlist
Radiation Tolerance	- TID dose > 100kRad(Si) - SEL LET$_{th}$ > 120 MeV-cm^2/mg - SEU rate < 10^{-10} #/bit/day at GEO orbit

Development and Validation	- Validation with TCAD simulation
	  - SEE mitigation design rules
	  - SEU/SET cross-section of DFF and clock buffers
	- Ground radiation tests
	  - no static SEU observed up to 10^7 cm^{-2} fluence
	  - further tests in progress

Embedded Two-Port SRAM

Category	Description
Foundry Process	- 0.13 um 1P8M CMOS - Epi-wafer not required - portable to similar foundry processes

Specifications	- Two-port (1R1W), intended applications:
	  - register file
	  - FIFO buffer
	- Organization: 512x22, scalable to 2048 x 39
	- Cell size: 5.14x1.33 um^2
	- Low operation voltage down to 0.7 V
	- Read access time
	  - 1.84 ns (input address registered)
	  - 1.25 ns (input address latched)

EDA Views	- Liberty (.lib) for synthesis - Verilog simulation model - LEF and Milkyway for P&R - GDSII layout - LVS netlist

Radiation Tolerance	- TID dose > 100kRad(Si)
	- SEL LET_{th} > 120 MeV-cm^2/mg
	- Internal registers hardened against SEU
	- Bit-cell raw SEU
	  - Threshold LET : 0.6 MeV-cm^2/mg
	  - Saturation cross-section : 2.0x10^{-8} cm^2
	- SEU mitigation:
	  - Compatible with SECDED EDAC
	  - Bit-interleaved layout (minimum bit distance > 20 um)

Design Capabilities

- Design Capabilities
  - Library development
  - Standard ASIC backend flow
  - Full-custom design
- On-going IP developments
  - Clock generator PLL
  - LVDS IO and SerDes
- Tapeout history (since 12/2013)
  - TID/SEE test vehicle
  - Controller ASIC
  - IEEE1394 link controller
  - Embedded SRAM/BIST test vehicle

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